CENTER OF NANOELECTRONICS & DEVICES

CND121: INTRODUCTION TO SILICON PROCESS & VLSI

Course Description:

The main objective of this course is to introduce the students to modern VLSI digital integrated circuit design and layout using CMOS technology with emphasis on "hands-on" IC design using CAD tools. The student will be using CAD tools for DRC, LVS, Layout editing, back annotation, and simulation. In addition, the student will be introduced to circuit optimization/circuit layout optimization in terms of timing, power, area, testability, and reliability.

Learning Outcomes

After successful completion of this course, the student will be able to:

- Design CMOS digital integrated circuits through a hands-on design process.
- Use a full-custom design flow to create complex CMOS digital integrated circuits
- Build a cell library to be used by other designs/designers and analyze circuits using both analytical and SPICE tools.
- Learn different parameters of full-custom design such as delay, power, area, reliability, and testability. Also, learn different circuit families (NMOS, CMOS, Pass gate, DCVSL,…) and the tradeoffs between these parameters in every family.
- Derive analytical circuit equations to estimate and compute the power efficiency of a VLSI design to prove designs meet specifications.
- Learn the full cycle of design starting from functional design, circuit design, and layout.

Lecture Schedule

- Introduction to Silicon Process & VLSI.
- The MOS(FET) Transistor.
- The CMOS inverter.
- Manufacturing CMOS ICs.
- Layout Design Rules.
- Designing Combinational Logic Gates - Static and Dynamic CMOS Design.
- Combinational Logic Gates – Layout.
- Designing Sequential Logic Gates in CMOS - Timing Metrics for Sequential Circuits, Static and Dynamic Latches and Registers.
- Pipelining: An Approach to Optimize Sequential Circuits.

Lab Sessions

Students will utilize Tanner EDA by Mentor Graphics to design and simulate and create the layout view, checking DRC, LVS verification and parasitic extraction for various CMOS digital integrated circuits such as MOSFETs, CMOS inverter and Logic Gates.

- **Lab 1**: Introduction to the flow of the Full Custom IC design cycle
  This lab is a general introductory tutorial to the flow of the Full Custom IC design cycle. Students will familiarize themselves with the Tanner EDA CAD tool.

- **Lab 2**: CMOS Inverter Design Schematic
  The objective of this lab is to characterize the NMOS & PMOS transistor by examining the "DC Sweep Analysis" and explore the IV behavior Simulation of NMOS & PMOS transistors.

- **Lab 3**: MOS Transistor Characterization
  In this experiment, we introduce the schematic design, symbol generation and testbench creation of the CMOS inverter. Students will also verify inverter functionality using Transient Analysis and characterize the CMOS inverter by examining the "DC Sweep Analysis".

- **Lab 4**: CMOS Inverter chain (Ring Oscillator) Design Schematic
  The Objective of this lab is to combine the CMOS inverter to build and simulate the Ring Oscillator. Students will also verify the Ring Oscillator functionality using Transient Analysis and understand the Frequency-Capacitance relationship. Capacitance tuning to generate frequencies like Digital & RF frequency will also be discussed.

- **Lab 5**: Inverter Layout Setup
  The objective of this lab is to build the layout for the inverter simulated in lab 3. Students will Place and Route (PnR) the CMOS Transistors to get the layout for the CMOS inverter and perform Design Rules Check (DRC). They will explore Layout vs Schematic (LVS) to verify layout and do Parasitic Extraction.

- **Lab 6**: Adder Design Schematic
  In this lab students will be introduced to designing combinational Logic Circuits. They will explore the Half Adder design and symbol generation. Full Adder design from the Half Adder symbol will be made. Students will also use bit stream generation to verify addition operation.

- **Lab 7**: Adder Layout Setup
  The objective of this lab is to build the layout of the 2-input NAND gate. Students will make Place and Route (PnR) for Adders and perform Design Rules Check (DRC). They will use Layout vs Schematic (LVS) to verify layout and do Parasitic Extraction.

- **Lab 8**: D Latch Design Schematic
  In this lab, students will be simulating the D latch. Students will be designing Sequential Logic Circuits. They will explore the D Latch design and symbol generation. They will also design a Flip Flop from the D Latch symbol and do Bit stream generation to verify functionality. Active Low/High Synchronous/Asynchronous design methodologies will also be explored.

- **Lab 9**: D Latch Layout Setup
  The main objective of this lab is to build the layout and check the DRC of the D latch. The students will do Place and Route (PnR) for D Latch and perform Design Rules Check (DRC). They will use Layout vs Schematic (LVS) to verify layout and do Parasitic Extraction.